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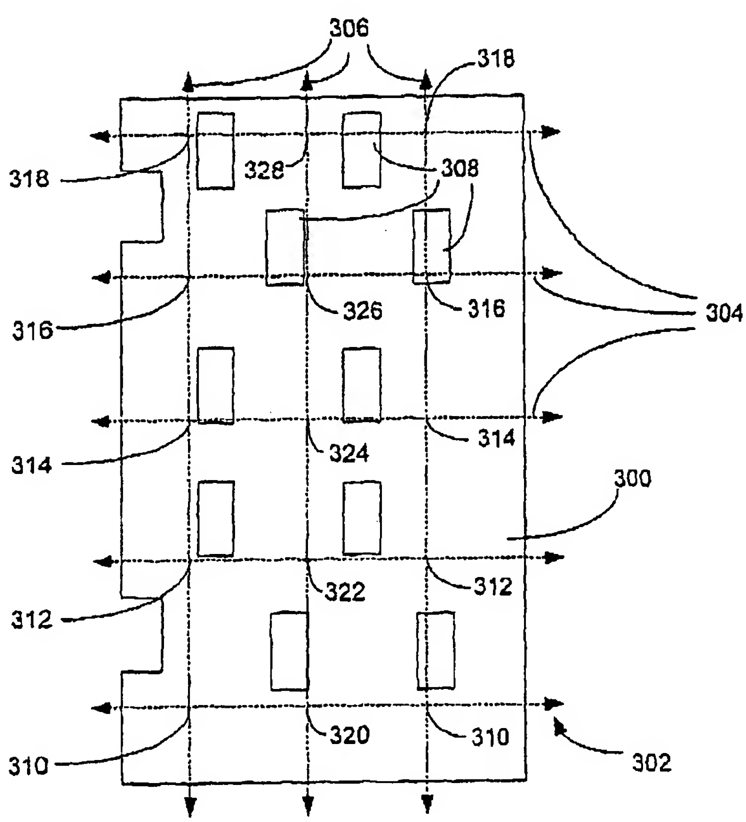
(54) Title: FIELD DECOUPLING CAPACITOR



(57) Abstract: An apparatus for decoupling a power plane from an electronic component on a printed circuit board includes a decoupling scheme comprised of a local and a remote component. The local component is comprised of a plurality of capacitors (500) disposed adjacent the electronic component (308) and configured to pass higher frequency signals. The remote component is comprised of a plurality of capacitors (214) disposed in a preselected pattern (304, 306) spaced from the electronic component and configured to pass middle and lower frequency signals.

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TITLE: FIELD DECOUPLING CAPACITOR

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

This invention relates generally to reducing noise in an electrical power supply, and, more particularly, to a method and apparatus for providing localized filtering of electrical power.

2. DESCRIPTION OF THE RELATED ART

Providing electrical power to electronic devices is becoming increasingly complex. Over time, voltage levels used to power various electronic devices have fallen dramatically. Many electronic components now operate at levels below 2 volts. As the operating voltage level has fallen, the sensitivity to variations in the voltage level has become more significant. That is, variations that were once insignificant, as compared to the overall voltage level, now constitute a significant percentage variation in the supplied voltage.

These variations, or noise, may lead to faulty operation of the electronic component. That is, an electronic component operating at 5 Volts nominally may be capable of tolerating a .2 Volt variation without adversely affecting the operation of the electronic component. However, when the voltage level of the electronic component is at 2 Volts, the same .2 Volt variation is a 10 percent deviation, which may cause unpredictable and/or improper operation of the electronic component.

Historically, these variations have been removed, or at least reduced, by adding decoupling capacitors to filter or otherwise smooth the voltage provided to the electronic components. Typically, these capacitors have been located adjacent the electronic components to which electrical power is being supplied. In some oases, the capacitors have been disposed on a printed circuit board extending about the periphery of an integrated circuit device. All other things being equal, the closer the capacitors are to the integrated circuit device, the more substantial the effect they have on the electrical power delivered thereto.

Typically, the decoupling capacitors have been selected to provide a relatively low impedance path within an expected frequency range. Far example, if an electronic component is expected to operate at about 200MHz, then the decoupling capacitors are selected to support a low inductance power distribution that encompass the 200MHz fundamental frequency as well as all of its associated harmonics out to about the fifth harmonic. In a typical application, several different fundamental frequency sources are used to clock different parts of the application. Today's applications frequently require a large selection of decoupling capacitors that provide low impedance decoupling from DC (0 Hz) to 1.5 GHz and beyond. Low impedance is, of course desired as it lowers the amount of power distribution noise, dynamic power consumed and heat generated.

Tantalum capacitors have been used in the past because they have a relatively wide frequency range in which low impedance operation occurs, Thus, a relatively small number of Tantalum capacitors are required to produce the overall low impedance frequency range (e.g.. 180-220 MHz). Multi-layer ceramic capacitors, however, lave begun to replace Tantalum capacitors in some applications. Multi-layer ceramic capacitors suffer from at least one significant disadvantage. That is, multi-layer ceramic capacitors have a relatively narrow frequency range in which low impedance operation occurs. Thus, a significantly greater number of multi-layer ceramic capacitors are required to provide the desired low impedance frequency range. Physically locating the required number of multi-layer ceramic capacitors adjacent the integrated circuit device has proven problematic.

SUMMARY OF THE INVENTION

In one aspect of the instant invention, a method is provided. The method is comprised of providing a power plane in a printed circuit board and mounting at least one electronic component on the printed circuit board coupled to the power plane. A decoupling scheme is then provided. The decoupling scheme comprises locating a first plurality of local capacitors adjacent the electronic component, and locating a second plurality of remote capacitors spaced from the electronic component.

In another aspect of the instant invention, an apparatus is provided. The apparatus is comprised of a printed circuit board, a power plane, at least one electronic component, and a decoupling scheme, The power plane is positioned within the printed circuit board. The at least one electronic component is positioned on the printed circuit board and coupled to the power plane. The decoupling scheme is comprised a remote component and a local component.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1 shows a stylized block diagram of a system in accordance with one embodiment of the present invention;

Figure 2 illustrates a stylized cross sectional view of a portion of a printed circuit board of the system of Figure 1;

Figure 3 illustrates a stylized top view of a printed circuit board of the system of Figure 1 in accordance with one embodiment of the present invention;

Figure 4 illustrates a stylized top view of a printed circuit board of the system of Figure 1 in accordance with another embodiment of the present invention;

Figures 5 illustrates a stylized top view of a portion of the printed circuit board of Figure 3 in a region adjacent an integrated circuit device; and

Figure 6 illustrates a stylized top view of an exemplary printed circuit board with exemplary capacitor values and spacing.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but, on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

Referring now to Figure 1, a block diagram of a system 110 in accordance with one embodiment of the present invention is illustrated. The system 110, in one embodiment, includes a plurality of system control boards 115(1-2) that are coupled to a switch 120. For illustrative purposes, lines 121(1-2) are utilized to show that the system control boards 115(1-2) are coupled to the switch 120, although it should be appreciated that, in other embodiments, the boards 115(1-2) may be coupled to the switch in any of a variety of ways, including by edge connectors, cables, or other available interfaces.

The system 110 includes a plurality of system board sets 129(1-n) that are coupled to the switch 120, as indicated by lines 150(1-n). The system board sets 129(1-n) may be coupled to the switch 120 in one of several ways, including edge connectors or other available interfaces. The switch 120 may serve as a communications conduit for the plurality of system board sets 129(1-n), half of which may be connected on one side of the switch 120 and the other half on the opposite side of the switch 120.

The switch 120, in one embodiment, may be a I8x18 crossbar switch that allows system board sets 129(1-n.) and system control boards 115(1-2) to communicate, if desired. Thus, the switch 120 may allow the two system control boards 115(1-2) to communicate with each other or with other system board sets 129(1-n), as well as allow the system board sets 129(1-n) to communicate with each other.

The system board sets 129(1-n), in one embodiment, comprise one or more boards, including a system board 130, I/O board 135, and expansion board 140. The system board 130 may include processors, as well as memories, ,for executing, in one embodiment, applications, including portions of an operating system. The I/O board 135 may manage I/O cards, such as peripheral component interface cards and optical cards that are installed in the system 110. The expander board 140, in one embodiment, generally acts as a multiplexer (e.g., 2:1 multiplexer) to allow both the system and I/O boards 130, 135 to interface with the switch 120, which, in some instances, may have only one slot for interfacing with both boards 130, 135.

The various boards 115(1-2), 120, 130, 135, 140 of the system 110 are generally comprised of printed circuit boards populated with a plurality of integrated circuit devices. The integrated circuit devices are electrically coupled to one another and to a source of electrical power so that they may perform their assigned tasks. This coupling is commonly accomplished via structures in the printed circuit boards on which the integrated circuits are mounted. A stylized cross sectional view of an exemplary portion of one of the printed circuit boards 200 of the system 10 is shown in Figure 2. The printed circuit board 200 is generally conventional in configuration, formed in a plurality of layers that may include various metallic traces or lines (not shown) and at least one power plane 202 and one ground plane 204. Generally, the power and ground planes 202, 204 extend throughout a significant portion of the printed circuit board 200, and operate to deliver electrical power to various components mounted on an upper surface 206 of the printed circuit board 200. For example, a conventional integrated circuit device 208 may be mounted on the upper surface 206 and have a plurality of electrically conductive pins 210, 212, which extend, at least partially, through the printed circuit board 200.

In the illustrated embodiment, the pin 210 extends through and is electrically coupled with the power plane 202. The pin 210 also extends through the ground plane 204 but is sufficiently separated therefrom such that no significant electrical coupling occurs between the ground plane 204 and the pin 210. Similarly, the pin 212 extends through and is electrically coupled with the ground plane 204. The pin 212 also extends through the power plane 202 but is sufficiently separated therefrom such that no significant electrical coupling occurs between the power plane 202 and the pin 212. In this manner, electrical power is supplied to the integrated circuit device 208 so that it may operate and perform its intended functions.

An exemplary decoupling capacitor 214 is similarly mounted on the upper surface 206 of the printed circuit board 200. A pair of leads 216, 218 extend from the capacitor 214 and through the printed circuit board 200, respectively engaging the power and ground planes 202, 204. Those skilled in the art will appreciate that the illustrated couplings are repeated at numerous locations throughout the printed circuit board 200 so as to distribute electrical power to the various components mounted thereon and to effectively remove undesirable variations in the electrical power delivered to these various components. In one embodiment of the instant invention, the positioning of the capacitors on the printed circuit board 200 may be used to enhance the effect of the capacitors.

Figure 3 illustrates a top view of one embodiment of a portion of a desired positioning scheme for decoupling capacitors on a printed circuit board 300. Generally, the positioning scheme has two components, a local component and a remote or shared component. Only the remote component of the positioning scheme is illustrated in Figure 3. A group of remote or shared decoupling capacitors are positioned on a grid 302 that encompasses a substantial portion of the printed circuit board 300. In the illustrated embodiment, the grid 302 covers the entire circuit board 300; however, it is envisioned that the grid 302 may be applied to less than the entire printed circuit board 300 without departing from the scope of the instant invention.

The grid 302 is composed of a plurality of horizontal and vertical lines, 304-306. The intersection of each of the horizontal and vertical lines 304, 306 represents a location at which a capacitor may be mounted. The locations identified by the intersections of the lines 304, 306 represent approximate locations at which the capacitors may be located. That is, in the event that the intersections of the lines 304, 306 coincide with components 308, such as integrated circuit devices, located on the printed circuit board 300, the position of the individual decoupling capacitors may be varied so that they remain near the location identified by the intersections of the lines 304, 306 but are spaced from the components 308. Alternatively, the entire grid 302 may be moved to reduce the number of locations falling on the component 308 on the printed circuit board 300.

Spacing between the lines 304, 306 may be varied according to several factors, such as the overall dimensions of the printed circuit board 300, the number of components 308 located on the printed circuit board 300, the current drawn or power consumed by the components 308, the voltage level applied to the power plane, etc. For example, where the overall dimensions of the printed circuit board 300 shown in Figure 3 are about 12.598 inches by about 2.283 inches, the spacing between the lines 304 is about 2.5 inches and the spacing between the lines 306 is about 1 inch. Those skilled in the art will appreciate that other spacing dimensions may be employed without departing from the scope of the instant invention.

The capacitors used in various embodiments of the instant invention may be generally characterized as falling within three groups - low, medium and high frequency. The individual capacitors are located on the printed circuit board using the positioning scheme described herein according to the group in which the individual capacitor falls. Generally, the high frequency capacitors are part of the local component of the positioning scheme. The middle and low frequency capacitors, on the other hand, are located within the remote or shared component of the positioning scheme, In one embodiment, where the fundamental frequencies that coexist in the same application fall within a range from 10MHz to 900MHz (i.e. 10 MHz, 33 MHz, 66 MHz, 75 MHz, 100MHz,150MHz, etc.), those capacitors having low impedance resonant frequencies in the rage of about 1 kHz to 500 kHz are considered to be low frequency decoupling capacitors, those having low impedance resonant frequencies in the range of about 500 kHz to 50 kHz are considered to be medium frequency decoupling capacitors, those having low impedance resonant frequencies in the range of about 50 kHz to 500 MHz are considered to be high frequency decoupling capacitors, and those having low impedance resonant frequencies in the range of about 500 MHz to 1.5 GHz and beyond are

considered to be ultra high frequency decoupling capacitors or EMI (electromagnetic radiation) capacitors. Those skilled in the art will appreciate that substantial variations in these exemplary ranges may be accomplished without departing from the scope of the instant invention.

In one exemplary embodiment, the values of the capacitors and the spacing of the grid may take on the values illustrated in Figure 6. Generally, close attention should be given to picking specific decoupling capacitors to ensure a relatively low ESL (equivalent series inductance) and ESR (equivalent series resistance). In some embodiments, it may be useful to use decoupling capacitors that have the absolute lowest ESL and ESR. The capacitor mounting inductance should also be reduced to a relatively low level, and in some embodiments it may be useful to minimize the capacitor mounting inductance. The field capacitance placement sequence and pattern, when used with the following general rules, provide a well balanced and flexible low impedance design across a very large frequency range.

1). The 22uF and the 100uF capacitors do most of the lower or bulk decoupling. The 22uF decoupling capacitors are known the foundational decoupling capacitors. The 22uF capacitors should be located with a significant density and symmetry, as compared to the other values. The 22uF capacitors should also be located at about every 2-5 grid points in a checkerboard fashion, especially concentrating on the areas where printed circuit board component density is greatest. The 100uF capacitors do not need to be used as heavily (*e.g.*, at about 1/5 the rate) as the number of 22uF capacitors, but still need to be assigned in an orderly and asymmetrical fashion.

2). The 10nF/4.7nF and 10nF/3.3nF combination decoupling capacitors directly address the fundamentals of 66, 75 and 100 MHz. These are also placed at about 1/2 the rate of the 22uF capacitors, as shown in Figure 6.

3) The 4.7nF and 1nF capacitors singly placed decoupling capacitors help bridge the field decoupling capacitors to the local decoupling capacitors by addressing the area of 80 MHz to 200MHz. These capacitors are to be assigned generally symmetrically closer to the local component decoupling capacitors at a rate of about 1/5 of that of the 22uF foundational decoupling capacitors.

Turning now to Figure 4, a top view of an alternative embodiment of a portion of a desired positioning scheme for decoupling capacitors on a printed circuit board 400 is shown. In this embodiment, the printed circuit board 400 includes a first and a second power plane (not shown) and, accordingly, two decoupling capacitor schemes, one scheme associated with each power plane. Generally, the positioning scheme for each power plane has two components, a local component and a remote or shared component. Only the remote component of the positioning schemes is illustrated in Figure 3. A group of remote or shared decoupling capacitors are positioned on the grid 302 and on a second grid 402, which both encompass a substantial portion of the printed circuit board 400. In the illustrated embodiment, the grids 302, 402 cover the entire circuit board 400; however, it is envisioned that the grids 302, 402 may be applied to less than the entire printed circuit board 400 without departing from the scope of the instant invention.

The grid 402, like the grid 302, is also composed of a plurality of horizontal and vertical lines 404, 406. The intersection of each of the horizontal and vertical lines 404, 406 represents a location at which a decoupling capacitor may be mounted. The locations identified by the intersections of the lines 304, 306 represent approximate locations at which the capacitors may be located. That is, in the event that the intersections of the lines 404, 406 coincide with components 308, such as integrated circuit devices, located on the printed circuit board 400, the position of the individual decoupling capacitors may be varied so that they remain near the location identified by the intersections of the lines 404, 406 but are spaced from the components 308. Alternatively, the entire grid 402 may be moved to reduce the number of locations falling on the components 308 on the printed circuit board 400.

Further, the spacing between the grids 302, 402 may be altered to reduce the number of locations falling on the components 308 on the printed circuit board 400.

Spacing between the lines 404, 406 may be varied according to several factors, such as the overall dimensions of the printed circuit board 400, the number of components 308 located on the printed circuit board 400, the current drawn or power consumed by the components 308, the voltage level applied to the corresponding power plane, etc. Those skilled in the art will appreciate that other spacing dimensions may be employed without departing from the scope of the instant invention.

Those skilled in the art will appreciate that the principles of the instant invention may be extended to cover any number of power planes contained within a printed circuit board. For example, a printed circuit board possessing three or more power planes may have three or more positioning scheme for decoupling capacitors located in remote and local configurations of the type described herein.

The local component of the positioning scheme for decoupling capacitors may be appreciated by reference to Figure 5. Figure 5 illustrates a top view of a portion of the printed circuit board 300 in a region surrounding one of the component 308. The local component is comprised of a plurality of capacitors 500 positioned adjacent the component 308. In the illustrated embodiment, the plurality of capacitors 400 is positioned surrounding the component 308. Generally, the local component of the decoupling scheme is made up of capacitors falling with the low frequency range.

The local capacitors 500 generally only have a significant affect an the component 308 to which they are adjacent. Capacitors positioned on the grid 302, however, have a significant affect on electrical power delivered to multiple ones of the components 308. That is, the capacitors on the grid 302 are "shared" among multiple components 308. This "sharing" of capacitors allows a single capacitor to positively affect the voltage level appearing at multiple components 308 on the printed circuit board 300. Thus, "sharing" capacitors allows fewer capacitors to be used to provide the desired level of filtering for each of the components 308.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above, may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

WHAT IS CLAIMED:

1. An apparatus, comprising:

a printed circuit board;

a power plane positioned within said printed circuit board;

at least one electronic component positioned on said printed circuit board and coupled to said power plane; and

a decoupling scheme, comprising:

a remote component; and

a local component.

2. The apparatus of claim 1, wherein the local component further comprises a plurality of capacitors positioned on the printed circuit board adjacent the electronic component, and the remote component further comprises a plurality of capacitors positioned on said printed circuit board and arranged in a preselected pattern spaced from the electronic component, wherein the capacitors are coupled to the power plane.

3. The apparatus of claim 2, wherein the preselected pattern is comprised of a plurality of crossing lines, with the capacitors being positioned near at least some intersections of the crossing lines.

4. The apparatus of claim 2, wherein the plurality of capacitors of the remote component include lower frequency capacitors, and the plurality of capacitors of the local component include higher frequency capacitors.

5. The apparatus of claim 2, wherein the plurality of capacitors of the remote component include lower and middle frequency capacitors, and the plurality of capacitors of the local component include higher frequency capacitors.

6. The apparatus of claim 1, further comprising a second power plane positioned within the printed circuit board, and wherein the decoupling scheme further comprises a second remote component, wherein the first remote component is associated with the first power plane and the second remote component is associated with the second power plane.

7. The apparatus of claim 2, further comprising a second power plane positioned within the printed circuit board, and wherein the decoupling scheme further comprises a second remote component, wherein the second remote component further comprises a plurality of capacitors positioned on said printed circuit board and arranged in a preselected pattern spaced from the electronic component, wherein the capacitors in the second remote component are coupled to the second power plane.

8. The apparatus of claim 7, wherein the preselected patterns of the first and second remote components is comprised of a plurality of crossing lines, with the capacitors being positioned near at least some intersections of the crossing lines.

9. The apparatus of claim 7, wherein the plurality of capacitors of the first and second remote components include lower frequency capacitors, and the plurality of capacitors of the local component includes higher frequency capacitors.

10. The apparatus of claim 7, wherein the plurality of capacitors of the first and second remote components include lower and middle frequency capacitors, and the plurality of capacitors of the local component includes higher frequency capacitors.

11. A method, comprising:

providing a power plane in a printed circuit board;

mounting at least one electronic component on the printed circuit board coupled to the power plane; and

providing a decoupling scheme, comprising:

locating a first plurality of local capacitors adjacent the electronic component; and

locating a second plurality of remote capacitors spaced from the electronic component.

12. The method of claim 11, wherein locating the second plurality of remote capacitors spaced from the electronic component further comprises locating the second plurality of remote capacitors in a preselected pattern of crossing lines, with the second plurality of capacitors being positioned near at least some intersections of the crossing lines.

13. The method of claim 11, wherein locating the first plurality of capacitors further comprises locating a first plurality of higher frequency capacitors adjacent the electronic component, and locating the second plurality of capacitors further comprises locating a second plurality of lower frequency capacitors spaced from the electronic component.

14. The method of claim 11, wherein locating the first plurality of capacitors further comprises locating a first plurality of higher frequency capacitors adjacent the electronic component, and locating the second plurality of capacitors further comprises locating a second plurality of lower and middle frequency capacitors spaced from the electronic component.

15. The method of claim 11, further comprising providing a second power plane, and wherein providing a decoupling scheme further comprises locating a third plurality of remote capacitors spaced from the electronic component.

16. The method of claim 15, wherein locating the third plurality of remote capacitors spaced from the electronic component further comprises locating the third plurality of remote capacitors in a preselected pattern of crossing lines, with the third plurality of capacitors being positioned near at least some intersections of the crossing lines.

17. The method of claim 16, wherein locating the third plurality of capacitors further comprises locating a third plurality of lower frequency capacitors spaced from the electronic component.

18. The method. of claim 11, wherein locating the third plurality of capacitors further comprises locating a third plurality of lower and middle frequency capacitors spaced from the electronic component.

19. An apparatus, comprising:

a printed circuit board;

a power plane positioned within said printed circuit board;

at least one electronic component positioned on said printed circuit board and coupled to said power plane; and

a decoupling scheme, comprising:

a remote component having a plurality of capacitors positioned on said printed circuit board and arranged in a preselected pattern spaced from the electronic component; and

a local component having a plurality of capacitors positioned on the printed circuit board adjacent the electronic component, wherein the capacitors are coupled to the power plane.

20. An apparatus; comprising:

a printed circuit board;

a power plane positioned within said printed circuit board;

at least one electronic component positioned on said printed circuit board and coupled to said power plane; and

a decoupling scheme, comprising:

a local component having a plurality of capacitors positioned on the printed circuit board adjacent the electronic component; and

a remote component having a plurality of capacitors positioned on said printed circuit board and arranged in a preselected pattern spaced from the electronic component, the pattern being comprised of a plurality of crossing lines, with the capacitors being positioned near at lest some intersections of the crossing lines.

21. An apparatus, comprising:

a printed circuit board;

a power plane positioned within said printed circuit board;

at least one electronic component positioned on said printed circuit board and coupled to said power plane; and

a decoupling scheme, comprising:

a local component having a plurality of local capacitors positioned on the printed circuit board adjacent the electronic component, the local capacitors being higher frequency capacitors; and

a remote component having a plurality of capacitors positioned on said printed circuit board and arranged in a preselected pattern spaced from the electronic component, the pattern being comprised of a plurality of crossing lines with the capacitors being positioned near at least some intersections of the crossing lines and being lower frequency capacitors.

22. An apparatus, comprising:

a printed circuit board;

a power plane positioned within said printed circuit board;

at least one electronic component positioned on said printed circuit board and coupled to said power plane; and

first means located adjacent the electronic component for decoupling the electronic component from the power plane; and

second means spaced from the electronic component for decoupling the electronic component from the power plane.

23. The apparatus of claim 22, wherein the first means further comprises passing a signal having a first higher frequency from the power plane to the electronic component, and the second means further comprises passing a signal having a second lower frequency from the power plane to the electronic component.

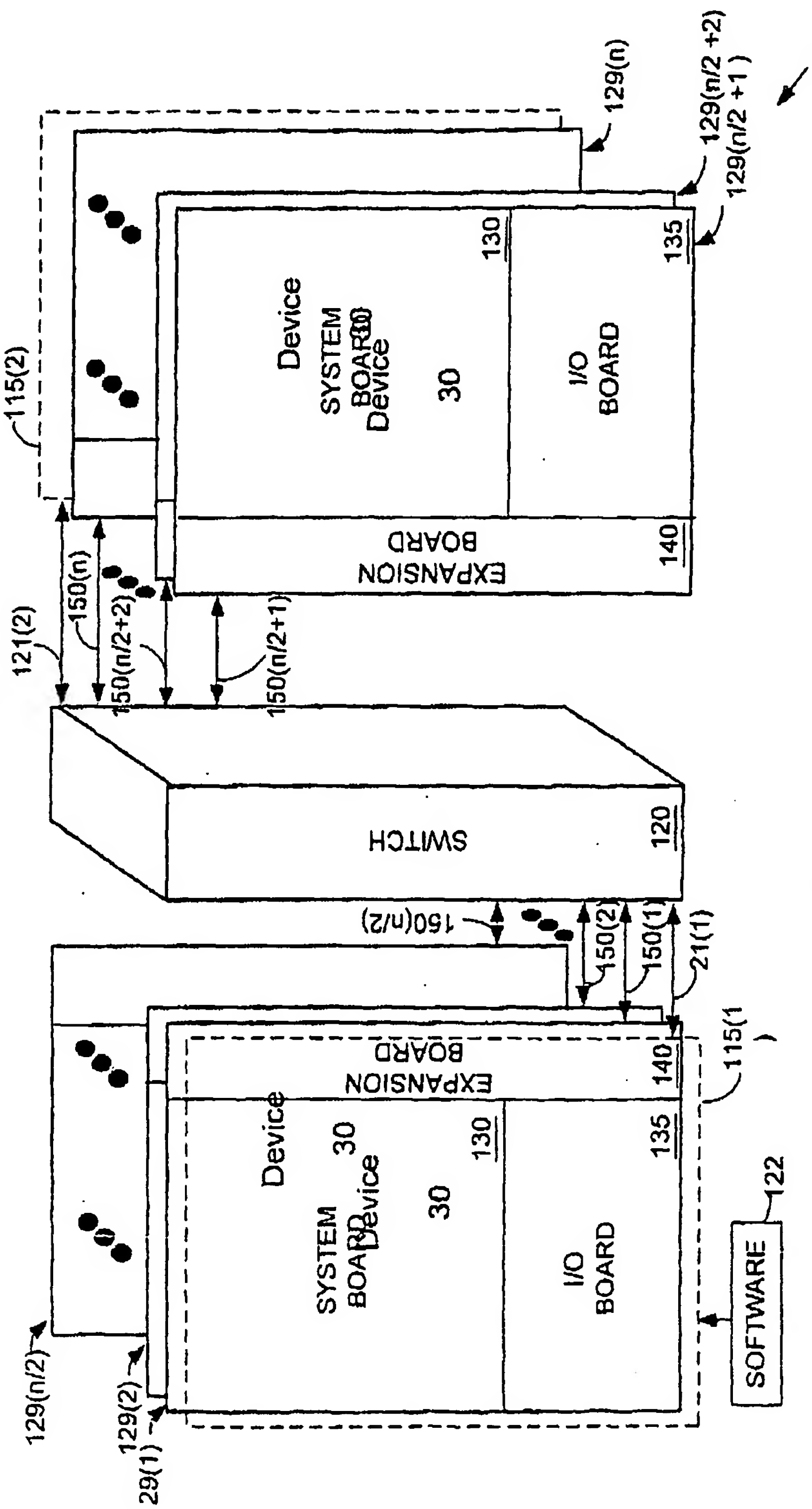
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Figure 1

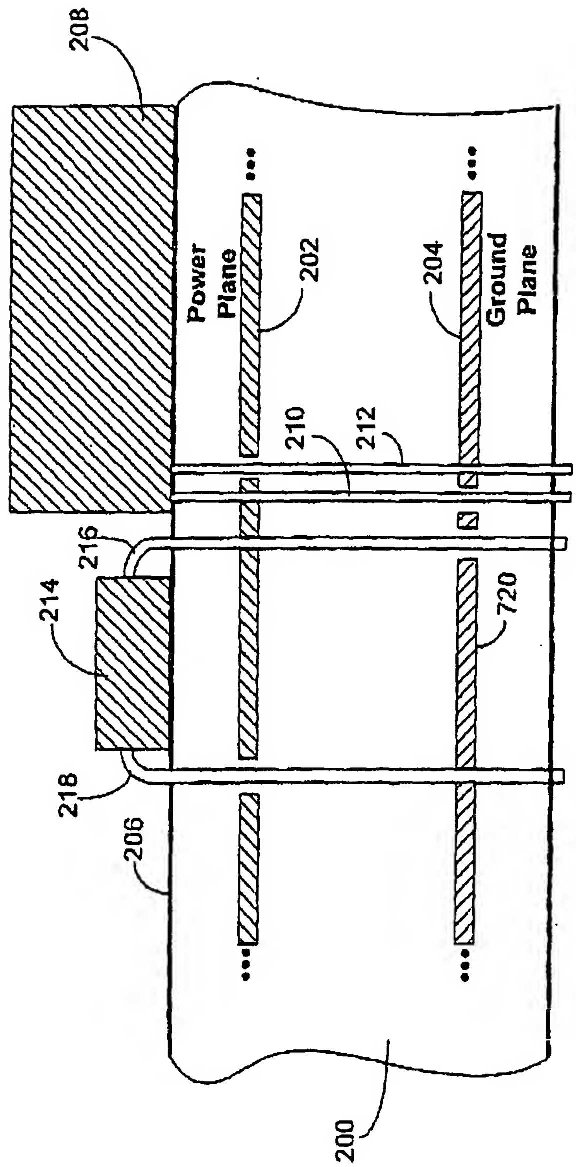
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Figure 2

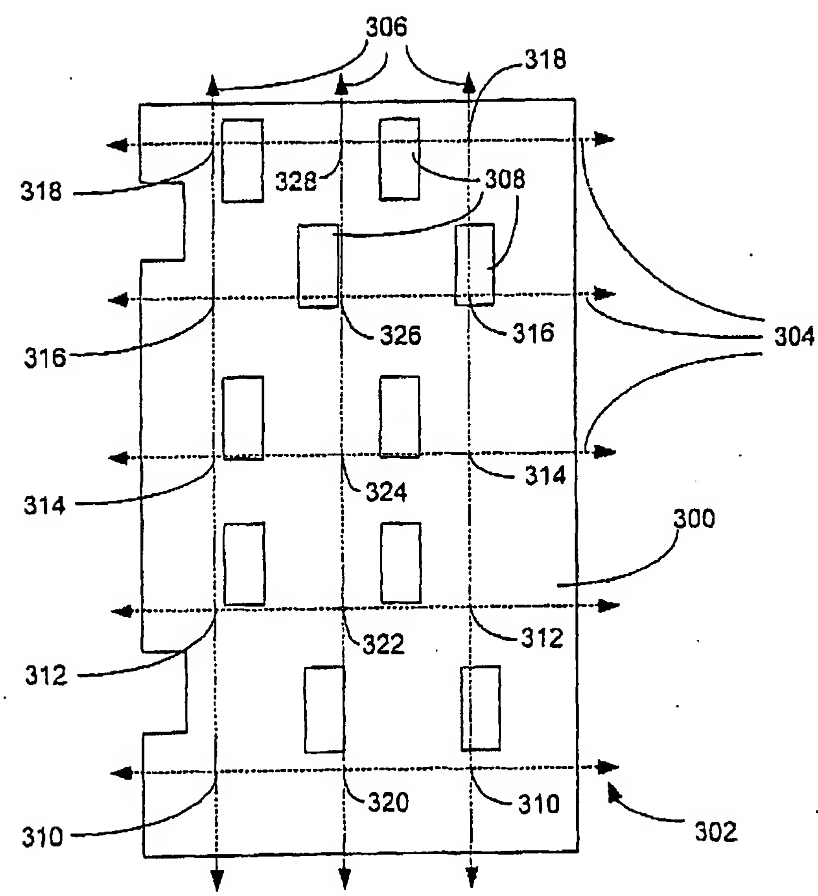
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Figure 3

Figure 4

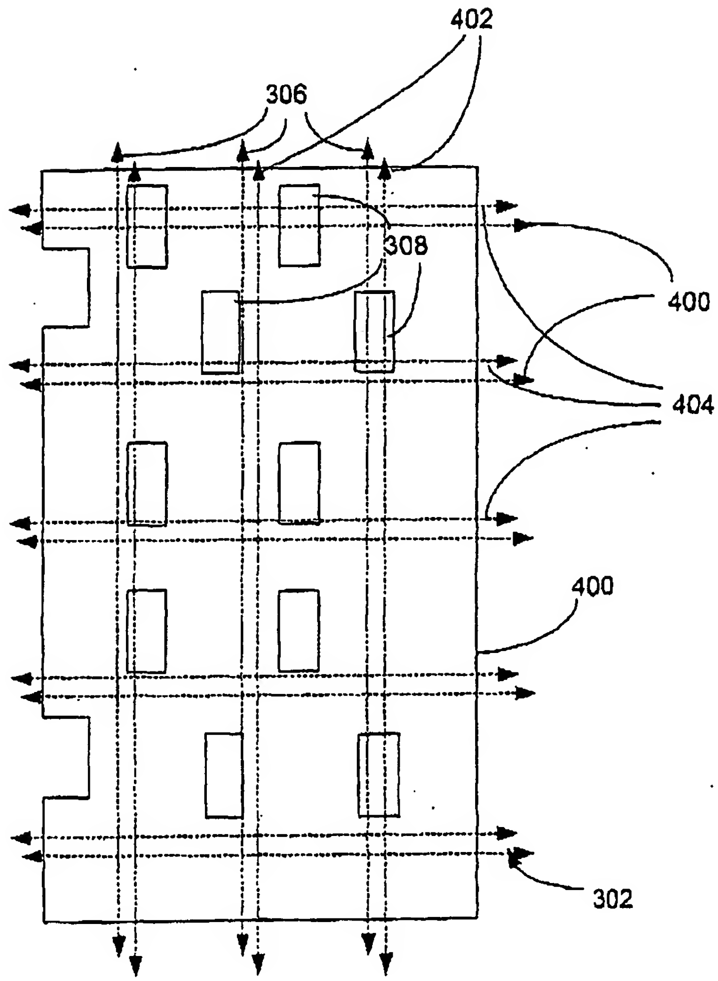
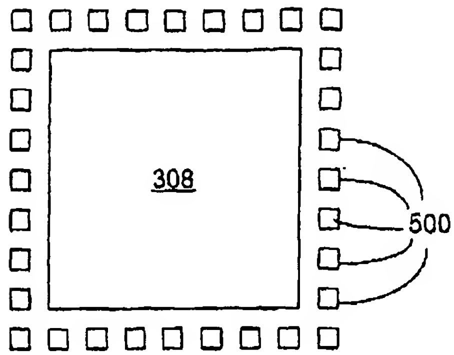


Figure 5



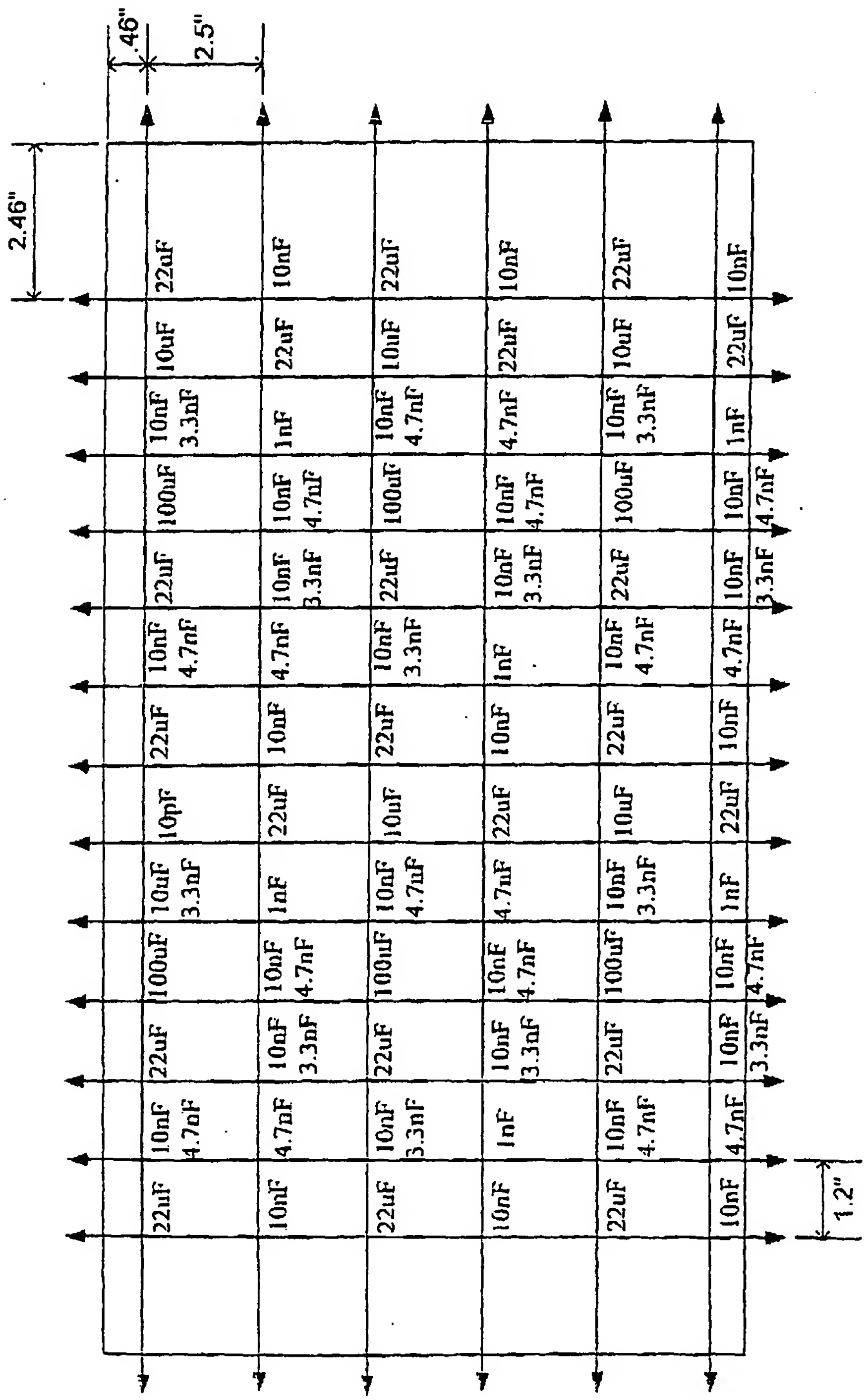


Figure 6

INTERNATIONAL SEARCH REPORT

Interna Application No
PCT/US 02/35431

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H05K1/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 104 258 A (NOVAK ISTVAN) 15 August 2000 (2000-08-15) the whole document ---	1-23
A	EP 0 472 317 A (AMERICAN TELEPHONE & TELEGRAPH) 26 February 1992 (1992-02-26) the whole document ---	1-23
A	WO 01 58224 A (INDUSTREE B V ;KOOLEN GERARDUS JOHANNES KAREL (NL)) 9 August 2001 (2001-08-09) the whole document -----	1-23

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
19 February 2003	27/02/2003

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INTERNATIONAL SEARCH REPORT

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